2-11-02



**PATENT** A

Docket No. CPH35726-D1

Date: February 07, 2002

J1025 U.S. PTO 02/07/02

JC978 U.S. PTO 10/072362 02/07/02

**ASSISTANT COMMISSIONER FOR PATENTS**
**WASHINGTON, D.C. 20231**

ATTENTION: APPLICATION BRANCH

Sir:

This is a request for filing a continuation application under 37 CFR 1.53 (b) **as a divisional application** of prior application No.**09/382,146** filed on **August 24, 1999.**

Prior application information: **Examiner: HU, SHOUZIANG ; Group Art Unit: 2811**

The entire disclosure of the prior application, from which an oath or declaration is supplied herewith as indicated below, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference.

Transmitted herewith for filing is the patent application of

Inventor(s): KUAN-YU FU ;

**For: MOSFET DEVICE**

Enclosed are:

(X) Specification in ( 12 ) pages.

(X) ( 8 ) sheets of drawings.

(X) Preliminary Amendment.

(X) A copy of Declaration and Power of Attorney from the prior application is enclosed.

(X) An executed Revocation of Power of Attorney signed by the Assignee.

(X) Return prepaid postcard.

**CLAIMS AS FILED**

| **FOR** | **NUMBER FILED** | **NUMBER EXTRA** | **RATE** | **FEE** |
|---|---|---|---|---|
| Basic Fee | | | \$ 740 | \$ 740 |
| Total Claims | 3 - 20 = 0 | × | \$ 18 | \$ 0 |
| Independent Claims | 1 - 3 = 0 | × | \$ 84 | \$ 0 |
| If application contains any multiple dependent claims(s), then add | | | \$ 280 | \$ 0 |
| **For a Large Entity:** | **TOTAL FILING FEE** | | | **\$ 740** |

(X) A check in the amount of \$740 to cover the filing fee is enclosed.

(X) The commissioner is authorized to charge any additional necessary fee to Account No. 50-0710 (Order No. CPH35726-D1). A duplicate copy of this sheet is enclosed.

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Registration No. 43,330

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Assistant Commissioner for Patents
Washington, D.C. 20231

**CERTIFICATE OF MAILING BY "EXPRESS MAIL"**

| | | |
|---|---|---|
| **Docket No.** | : | **CPH35726-D1** |
| **Inventor(s)** | : | **KUAN-YU FU** |
| **For** | : | **MOSFET DEVICE** |
| **"Express Mail" Mailing Label No.** | : | **EV 016848514 US** |
| **Date of Deposit** | : | **February 07, 2002** |

I hereby certify that the accompanying

Transmittal in Duplicate; Specification in 12 page(s); 8 sheet of drawing(s); Copies of Declaration and Power of Attorney from prior application; Revocation of Power Attorney; Preliminary Amendment; Checks for Filing Fee(s); Return Prepaid Postcard

are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and are addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

M. Chang

Michelle Chang

**PATENT** Docket No.:CPH35726-D1

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | | |
|---|---|---|
| Applicant: | KUAN-YU FU et al. | ) |
| Filed: | Herewith | ) |
| For: | MOSFET DEVICE | ) |
| | | ) |

## PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Prior to the examination on merits, please amend the above-identified application as follows:

**IN THE TITLE:**

Please change the title to read:

--MOSFET DEVICE--

**IN THE SPECIFICATION:**

Please add the following paragraph on page 1, after line 2.

--CROSS-REFERENCE TO RELATED APPLICATION

This application is a divisional application of, and claims the priority benefit of, U.S. application serial No. 09/382,146 filed on August 24, 1999, which in term is a divisional applicaion of U.S. Patent application No. 09/059,548, filed on April 13, 1998.--

**IN THE CLAIMS:**

Please cancel claims 1-9 without prejudice and disclaimer.

Please add the following new claims 10-12:

10. A semiconductor structure comprising a substrate having an active region of a first conductivity type including a channel region and a non-channel region surrounding the channel

region, at least a first trench and a second trench disposed in the channel region, the structure comprising:

a thick insulating layer disposed over the said first and second trench, the thick insulating layer being conformal to the said first and second trench profile;

a gate electrode disposed over the said first and second trenches, the gate electrode comprising a first vertical portion, a second vertical portion and a horizontal portion, wherein the first vertical portion being embedded inside the first trench, the second vertical portion being embedded inside the second trench, and the horizontal portion being disposed over the substrate and connecting the said first and second portions together; and

a first shallow doped region within the substrate disposed at an upper corner adjacent to the first vertical portion and a second shallow doped region disposed at an upper corner adjacent to the second vertical portion of the electrode; and

a first deep source/drain junction region extending from the first shallow doped region, and a second deep source/drain junction region from the second shallow doped region, wherein the first and second deep source/drain junction regions are disposed in a region within the substrate deeper than the first and second trench.

11. The structure according to claim 10, wherein the thick insulating layer is formed by thermal oxidation.

12. The structure according to claim 10, wherein the thickness of the thick insulating layer is about 0.1 μm.

Respectfully submitted,

Dated: 2/7/2002

By: ______

Jiawei Huang
Registration No. 43,330

**Correspondence Address:**
**4 Venture, Suite 250**
**Irvine, California 92618**
**(949) 660-0761**

## VERSION WITH MARKINGS TO SHOW CHANGES MADE

**IN THE TITLE:**

The title has been amended as follows:

MOSFET DEVICE [AND METHOD OF FABRICATING THE SAME BACKGROUND OF THE INVENTION]

# MOSFET DEVICE AND METHOD OF FABRICATING THE SAME

## BACKGROUND OF THE INVENTION

### Field of the Invention

The invention relates in general to a multiple T-shaped gate MOSFET device, and more particularly to a MOSFET device, which can increase the ICs' density and speed without physically scaling down the device's channel length and width.

### Description of the Related Art

In the process of fabricating a MOSFET device, in order to scale down the device, both the channel width and length dimensions are shortened. As the attempt to increase the ULSI device density and speed continues, the technology in the deep sub-micron regime becomes more and more difficult so that it eventually may reach a theoretical limitation. As a result, it is impossible to limitlessly increase the device's density and speed. In addition, the short channel effect will render the technology even more prohibitive. For example, as the channel width and the length dimensions are shortened, punch through of the carriers and the hot carrier effect occur. When the device is even more scaled down, the short channel effect becomes especially significant.

Figures 1A to 1H are schematic, cross-sectional views of conventional MOSFET device formation processes. Referring to Figure 1A, a device includes a substrate 100, a pad oxide layer 102, a silicon nitride layer 104, and a photoresist layer 106. A mask 108 is used to pattern the device. Referring to Figure 1B, a trench 107 is formed in the

substrate 100 by defining the photoresist layer 106, the silicon nitride layer 104, the pad oxide layer 102 and the substrate 100.

The remainder of the photoresist layer 106a and the silicon nitride layer 104a are removed to expose the remainder of the pad oxide layer 102a, as shown in Figure 1C. Referring to Figure 1D, a dielectric layer 110 is formed in the trench 107 and over the substrate 100. The dielectric layer 110 is polished to expose the substrate 100 and form a shallow trench isolation (STI) structure 110a as shown in Figure 1E. Then, a gate oxide layer 112, a metal layer 114, and a photoresist layer 116 are formed on the substrate in turn. Next, a mask 118 is further used to pattern the device.

A gate 114a is formed on the substrate 100 by defining the photoresist layer 116, the metal layer 114, and the gate oxide layer 112 as shown in Figure 1F. Then, the substrate 100 is implanted with ions to form a shallow doped region 111 in the substrate 100. Referring to Figure 1G, an oxide layer 120 is deposited on the substrate 100. Then, the oxide layer 120 is etched to form spacers 120a besides the gate 114a by dry etching as shown in Figure 1H. Then, the substrate 100 is implanted with ions to form a deep doped region 113.

The technology will reach a limit in developing high integrity and operating rate. When the device becomes smaller the short channel effect becomes especially apparent.

The references regarding changing the gate shape to increase the integrity and the operating rate are:

1. F.E. Holmes and C.A.T Salama, Solid State Electron, 17.791 (1974) for V-

shape MOS.

2. C.A.T Salama, Solid State Electron, 20.1003 (1977) for U-shape MOS.

## SUMMARY OF THE INVENTION

It is therefore an object of the invention to provide an improved resolution to the conventional MOSFET device. Using a multiple T-shaped gate (utilizing the trench technology), device density and speed can be increased without physically scaling down the MOSFET's channel length and width. Once this approach is adopted in the effort to miniature ULSI devices, the short channel effect will be of much less concern.

It is another object of the invention to provide a MOSFET with multiple T-shaped gate, wherein the gate length is increased to improve the operating rate and the integrity.

The invention achieves the above-identified objects by providing a new method of fabricating a MOSFET with a multiple T-shaped gate. The fabricating method includes the following steps. A substrate with an active region and a non-active region is provided. A plurality of trenches are formed in both the active region and the non-active regions in the substrate. An insulating layer is formed in the trenches. The insulating layer in the trenches of the active region is etched. A thin insulating layer is formed in the trenches of the active region and over the surface of the substrate. A conducting layer is formed in the trenches of the active region. The conducting layer is defined to form a gate. The device is implanted with first ions. Then, the device is further implanted with second ions by using a mask, wherein the mask expose the trenches of the active region, and the opening of the mask is wider than the trench.

The MOSFET device includes at least the following structures. A substrate includes an active region and a non-active region, wherein the active region includes a plurality of trenches and the non-active region includes a plurality of shallow trench isolation structures. A thin insulating layer is formed in the trenches of the active region and over the substrate. A multiple T-shaped gate is formed with a first part and a second part, wherein the first part is formed between two trenches on the substrate, and the second part is formed in the trenches of the active region. A source/drain region includes a shallow doped region and a deep doped region, wherein the shallow doped region is in the substrate under the first part, and the deep doped region is in the substrate besides the second part.

## BRIEF DESCRIPTION OF THE DRAWINGS

Other objects, features, and advantages of the invention will become apparent from the following detailed description of the preferred but non-limiting embodiments. The description is made with reference to the accompanying drawings in which:

Figures 1A to 1H (Prior Art) are cross-sectional views showing a conventional process of forming a gate;

Figures 2A to 2F are cross-sectional views showing the process steps of the method for fabricating a multiple T-shaped gate MOSFET device in accordance with a preferred embodiment of the present invention;

Figures 3A to 3B are the top views of the MOSFET device as shown in Figure 2F and 2G; and

Figures 4A to 4D are cross-sectional views of a multiple T-shaped gate MOSFET device in accordance with the preferred embodiment.

## DESCRIPTION OF THE PREFERRED EMBODIMENT

In accordance with the preferred embodiment of the present invention, a multiple T-shaped gate MOSFET device is provided to increase the operating rate of the ICs and to lower the short channel effect in high integrity ICs. Figure 2A to 2G are cross-sectional views showing the process steps of one preferred embodiment for fabricating a two T-shaped gate MOSFET device.

Referring first to Figure 2A, a substrate 200 is provided, wherein a number of trenches 201 are formed in the substrate 200. A dielectric layer is formed in the trenches 201 and over the substrate 200 by chemical vapor deposition (CVD). Then, the dielectric layer is polished to expose the surface of the substrate 200 and form several shallow trench isolation (STI) structures 202 as shown in Figure 2B. The device includes an active region 203 and a non-active region 205.

Referring to Figure 2C, a mask 204 is used to pattern the STI structures 202 of the active region 203. The STI structures 202 of the active region 203 are etched to expose the trenches 201 and leave the remainder of the dielectric layer 202a on the sides of the trenches 201. The STI structures 202 are used to isolate the MOSFET device.

Referring to Figure 2D, a thin dielectric layer is formed in the trenches 201 and over the substrate 200. The thin dielectric layer formed in the trenches 201 is a side-wall oxide layer 202a and over the substrate 200 is a gate oxide layer 206. The thickness of

the side-wall oxide layer 202a is about 0.1μm. The side-wall oxide layer 202a is used to protect the device from generating parasitic capacitance. Then, a conducting layer 208 is formed on the device by CVD as shown in Figure 2E.

Referring to Figure 2F, the conducting layer 208 is patterned to form a gate 209. The gate 209 includes a first gate part 209a and a second gate part 209b, wherein the first gate part 209a lies on the substrate 200 between the trenches 201 and the second gate part 209b is in the trenches 201 of the active region 203. Then, the device is implanted to form a number of shallow doped regions 212 in the substrate 200 of the active region 203.

Referring to Figure 2G, the device is further implanted to form a number of deep doped regions 216 by using a mask 214, wherein the mask 214 is used to expose the trenches 201 of the active region 203. The opening of the mask 214 is wider than the trench 201.

Figure 3A is the top view of the MOSFET device as shown in Figure 2F and Figure 3B is the top view of the MOSFET device as shown in Figure 2G. Figure 3A includes the shallow doped region 212 and the gate 209. Figure 3B includes the deep doped region 216, the shallow doped region 212 and the gate 209.

Figures 4A to 4D show a three T-shaped gate MOSFET device in accordance with the preferred embodiment. Figure 4A shows a top view of the three T-shaped gate MOSFET device. In Figure 4A, the device includes a gate 300, a shallow doped region 304, a deep doped region 306, and an oxide layer 302.

Figure 4B shows the cross-sectional view taken along the line AA' of the Figure 4A. As Figure 4B shows, the device includes a substrate 308, the gate 300, the oxide layer 302 and STI structures 312. W denotes the channel width of the device.

Figure 4C shows the cross-sectional view taken along the line BB' of the Figures 4A and 4B. As Figure 4C shows, the device includes the substrate 308, the gate 300, the shallow doped region 304, and a gate oxide layer 310 under the gate 300, wherein L denotes the channel length of the device.

Figure 4D shows the cross-sectional view taken along the line CC' of the Figures 4A and 4B. As Figure 4D shows, the device includes the substrate 308, the gate 300, the shallow doped region 304, and the deep doped region 306. For the device, the shallow doped region 304 and the deep doped region 306 form the source/drain regions.

The preferred embodiment discloses a multiple T-shaped gate MOSFET device. The device has "gate legs" dipped into the trenches in the substrate. Between the "gate legs" in the trenches and the source/drain junctions, a thicker dielectric layer (>0.1μm) is formed to reduce parasitic capacitance. Around the dielectric layer (~0.1μm in the horizontal dimension), the source/drain junctions are doped to a depth as deep as the trench to create the transistor action under the bottom as well as at the side walls of the trench. With this special structure, the transistor's width is effectively increased by $2nt$, wherein $n$ is the number of trenches and $t$ is the trench depth. This requires 2 extra masks in the process: one for the dielectric etch in the trenches (mask 204 in Figure 2C) and another for the deep source/drain junction implant (mask 214 in Figure 2G). The value of the advantages gained by this invention should exceed the price of the extra

mask(s). The effective width of the transistor is increased by $2nt$, while the real surface dimension can be reduced. For example, if both the trench width and space are 0.5μm and t is 1μm, the reduction in the linear dimension of ULSI circuits will be 50%. With this approach, instead of continuing the scaled-down of both W and L in MOSFET, one can increase $n$ and $t$ to achieve the same purpose, i.e., to increase density and speed. The short channel effect will be of much less concern in this approach.

While the invention has been described by way of example and in terms of a preferred embodiment, it is to be understood that the invention is not limited thereto. To the contrary, it is intended to cover various modifications and similar arrangements and procedures, and the scope of the appended claims therefore should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements and procedures.

WHAT IS CLAIMED IS:

1. A method of fabricating a MOSFET device, comprising the steps of:

providing a substrate, the substrate including an active region and a non-active region;

forming a plurality of trenches;

forming a dielectric layer in the trenches;

removing the dielectric layer in the trenches of the active region;

forming a thin insulating layer in the trenches of the active region and over the substrate;

forming a conducting layer in the trenches of the active region and over the substrate;

patterning the conducting layer to form a gate layer;

implanting the substrate with first ions; and

implanting the substrate with second ions by using a mask, wherein the mask exposes the trenches of the active region, and the opening of the mask is wider than the trench.

2. A method according to claim 1, wherein the dielectric layer is formed by CVD.

3. A method according to claim 1, wherein the thin oxide layer is formed by thermal oxidation.

4. A method according to claim 1, wherein the thickness of the thin oxide layer is about 0.1μm.

5. A method according to claim 1, wherein the conducting layer is formed by CVD.

6. A method according to claim 1, wherein said step of implanting the substrate with first ions is to form a shallow doped region.

7. A method according to claim 1, wherein said step of implanting the substrate with second ions is to form a deep doped region.

8. A MOSFET device, comprising:

a substrate, wherein the substrate includes an active region and a non-active region, and the substrate includes a plurality of trenches;

a plurality of shallow trench isolation structures, wherein the shallow trench isolation structures are in the trenches of the non-active region;

a thin insulating layer, formed in the trenches of the active region and over the surface of the substrate;

a multiple T-shaped gate layer, including a first part and a second part, wherein the first part is on the surface between two trenches, and the second part is in the trenches

of the active region; and

a source/drain region, including a shallow doped region and a deep doped region, wherein the shallow doped region is in the substrate under the first part, and the deep doped region is in the substrate besides the second part;

wherein the deep doped region is deeper than the trenches, and the trenches are deeper than the shallow doped region.

9. A MOSFET device according to claim 1, wherein the thin insulating layer on side-walls of the trenches is about 0.1μm.

* * * * *

## ABSTRACT OF THE DISCLOSURE

A method of fabricating a MOSFET device with a multiple T-shaped gate has the following steps. A substrate with an active region and a non-active region is provided, wherein the active region has a plurality of trenches, and the non-active region has a plurality shallow trench isolation structures. A thin insulating layer and a conducting layer are formed in the trenches. The conducting layer is defined to form a gate. The device is implanted with first ions. Then, the device is further implanted with second ions by using a mask, wherein the mask expose the trenches of the active region, and the opening of the mask is wider than the trench. The MOSFET device has at least the following structures. There is a substrate with an active region and a non-active region, wherein the active region has a plurality of trenches and the non-active region has a plurality of shallow trench isolation structures. There is a multiple T-shaped gate with a first part and a second part, wherein the first part is formed between two trenches on the substrate and the second part is formed in the trenches of the active region. There is a source/drain region with a shallow doped region and a deep doped region. The multiple T-shaped gate increases the channel width of the MOSFET device and decreases the short channel effect of the high integrity ICs.

* * * * *

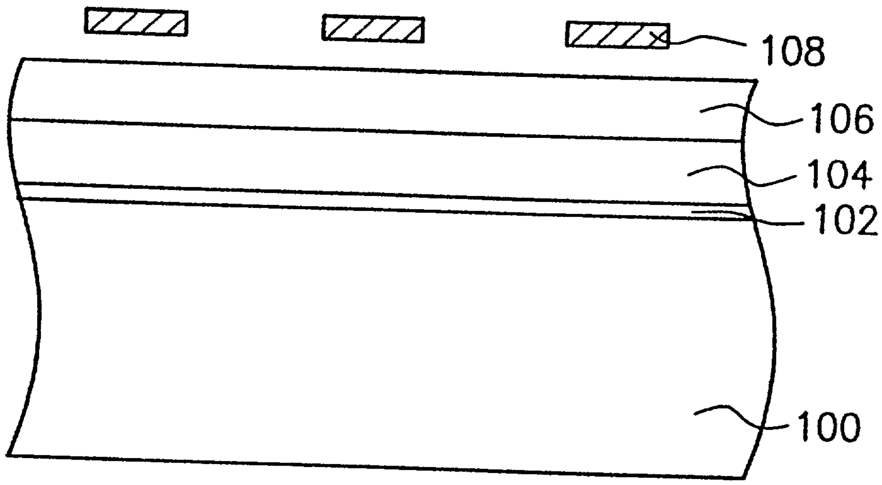


FIG. 1A (PRIOR ART)

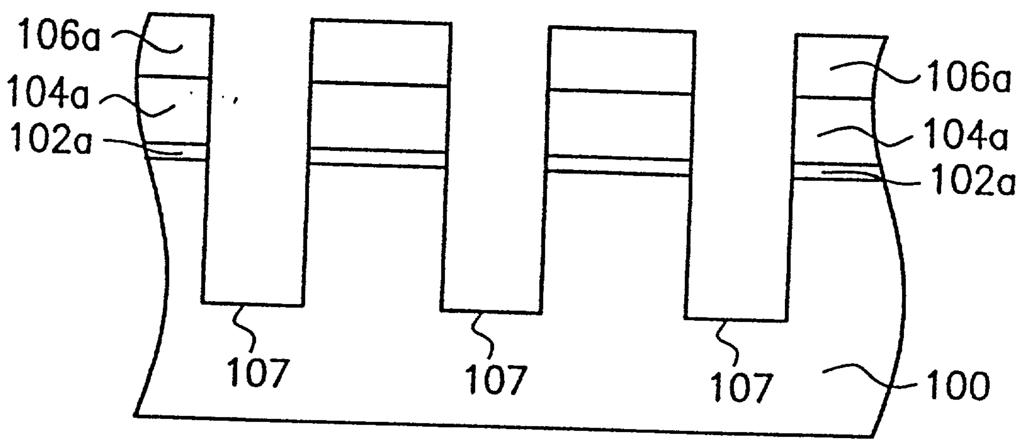


FIG. 1B (PRIOR ART)

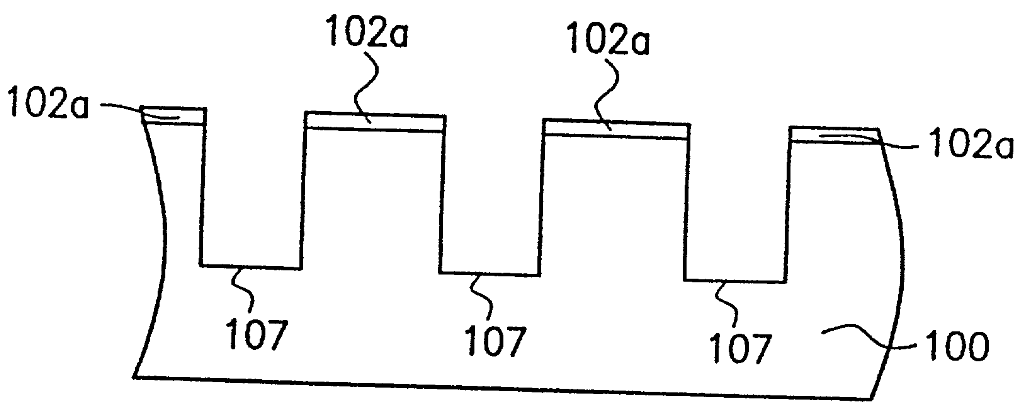


FIG. 1C (PRIOR ART)

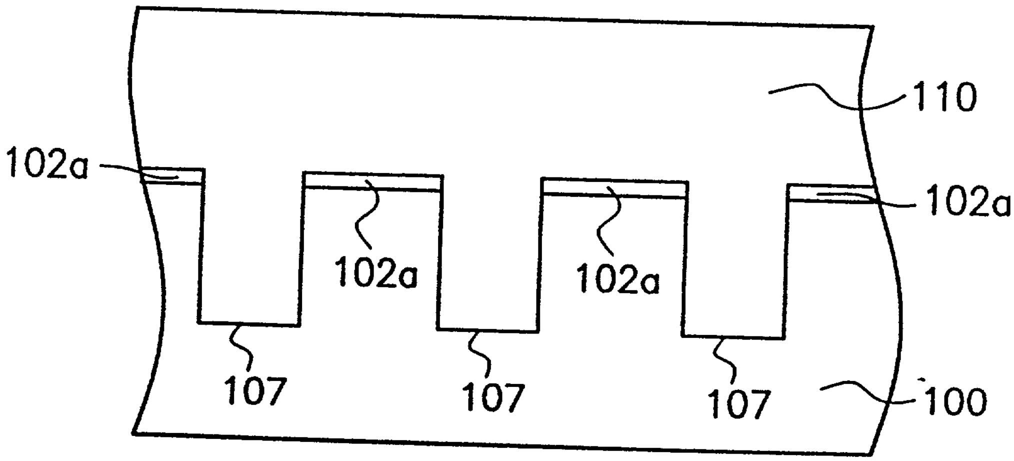


FIG. 1D (PRIOR ART)

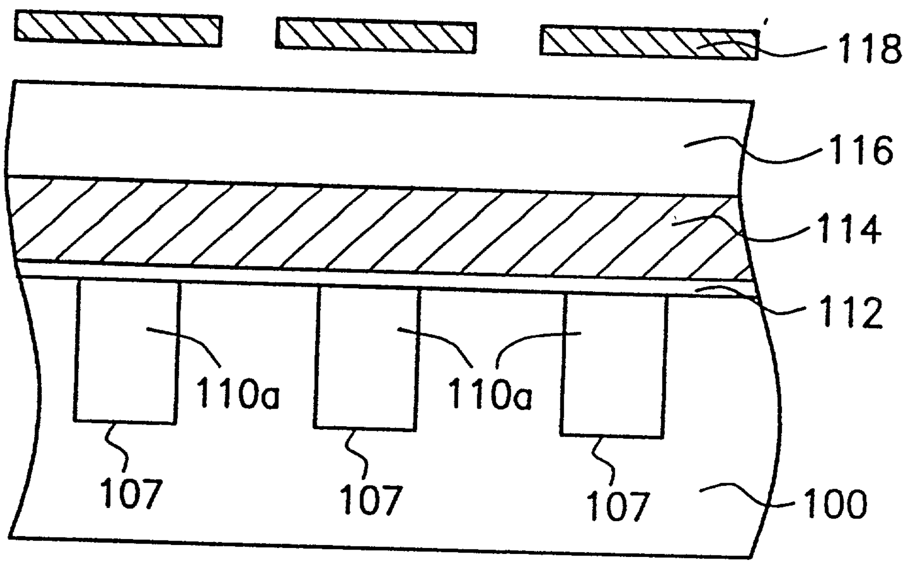


FIG. 1E (PRIOR ART)

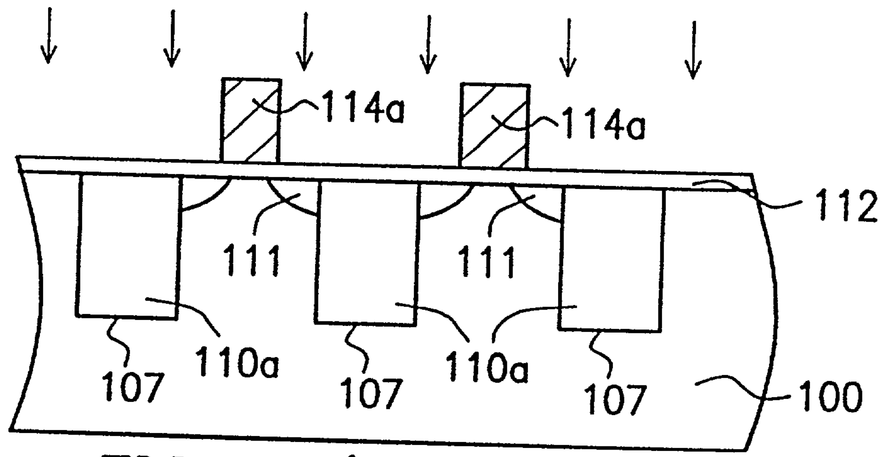


FIG. 1F (PRIOR ART)

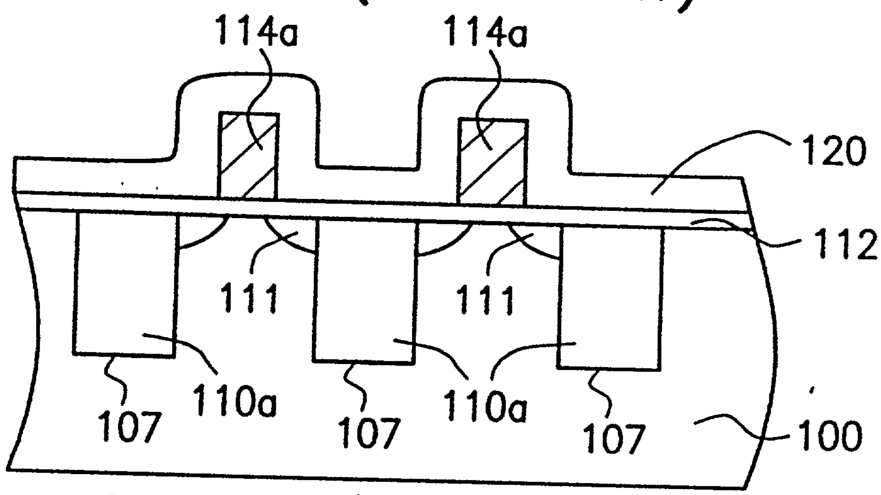


FIG. 1G (PRIOR ART)

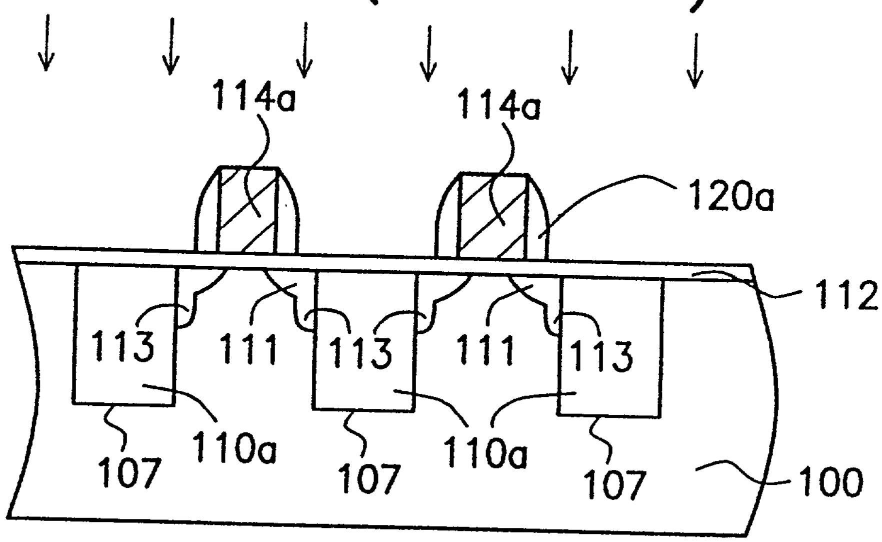


FIG. 1H (PRIOR ART)

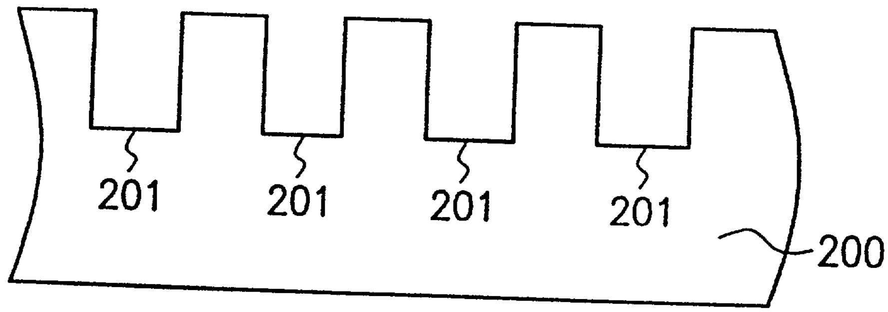


FIG. 2A

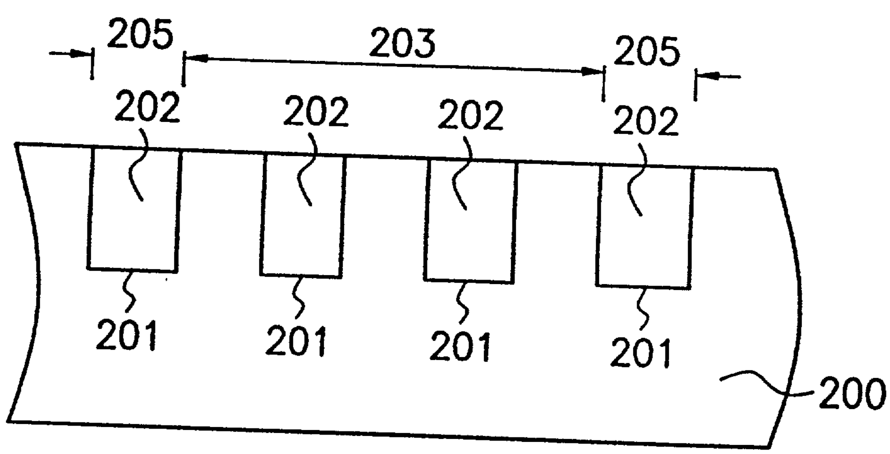


FIG. 2B

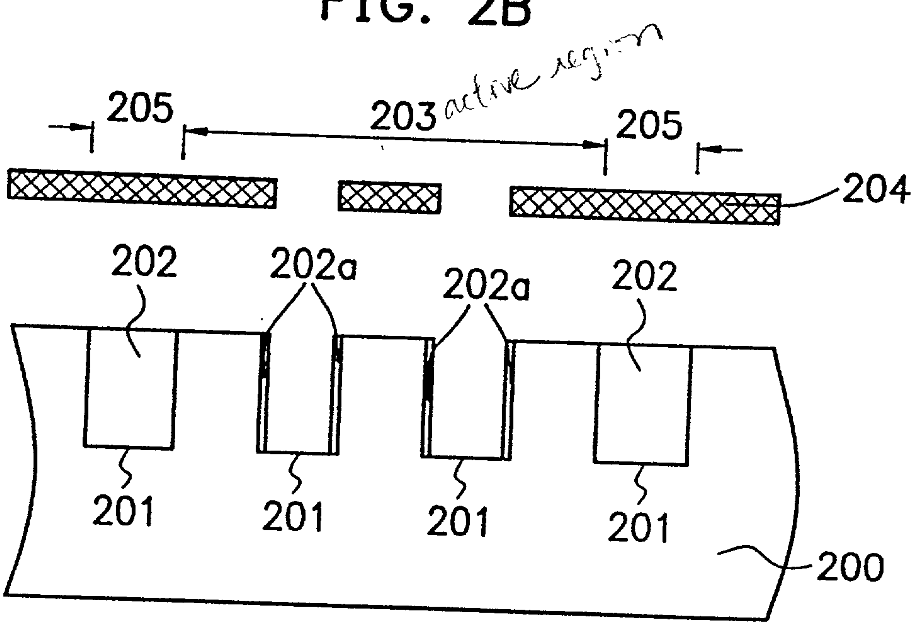


FIG. 2C

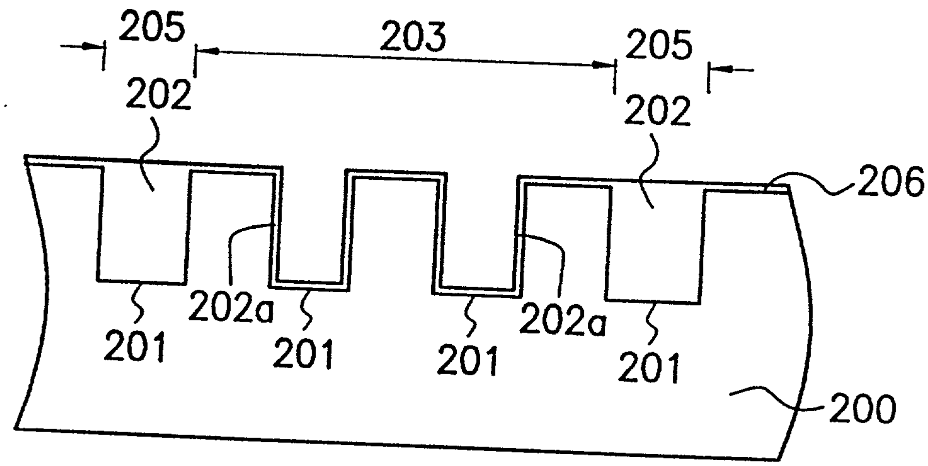


FIG. 2D

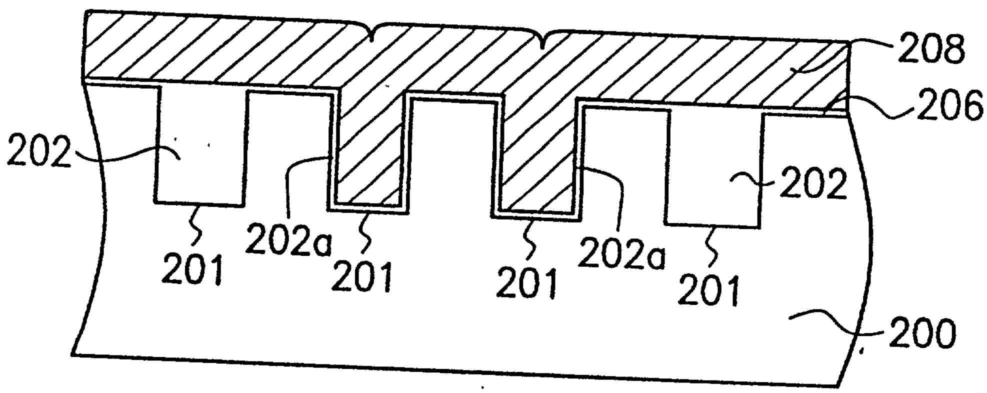


FIG. 2E

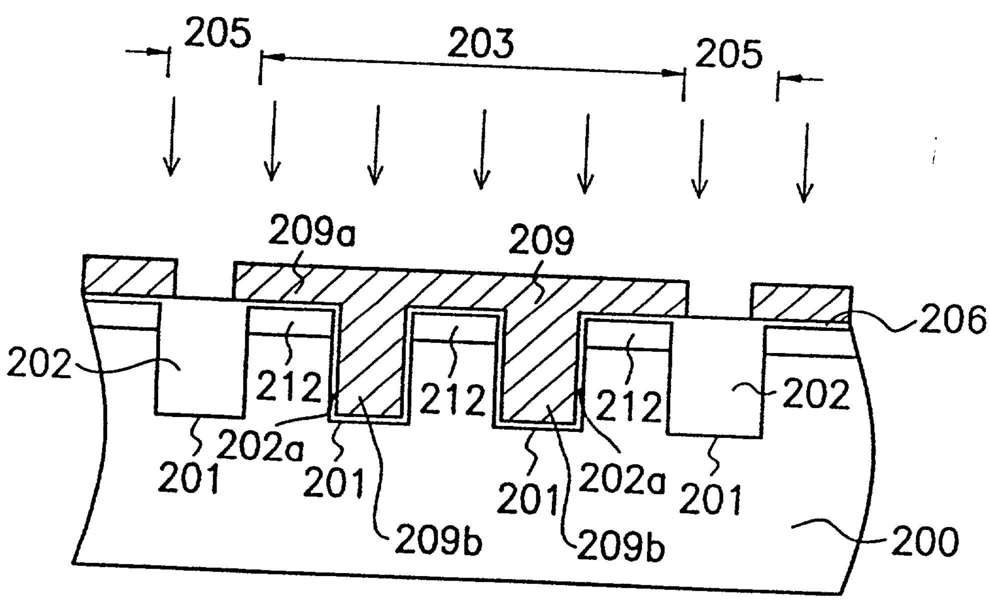


FIG. 2F

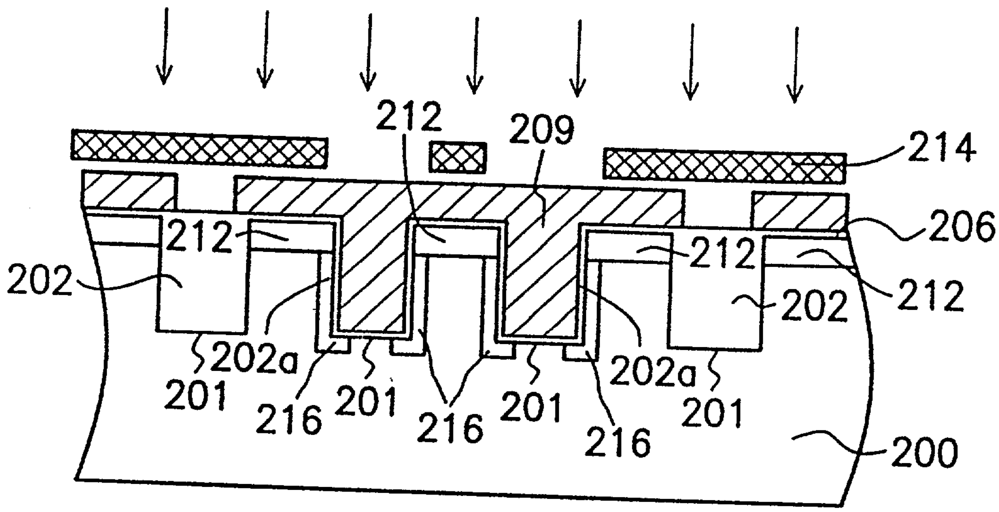


FIG. 2G

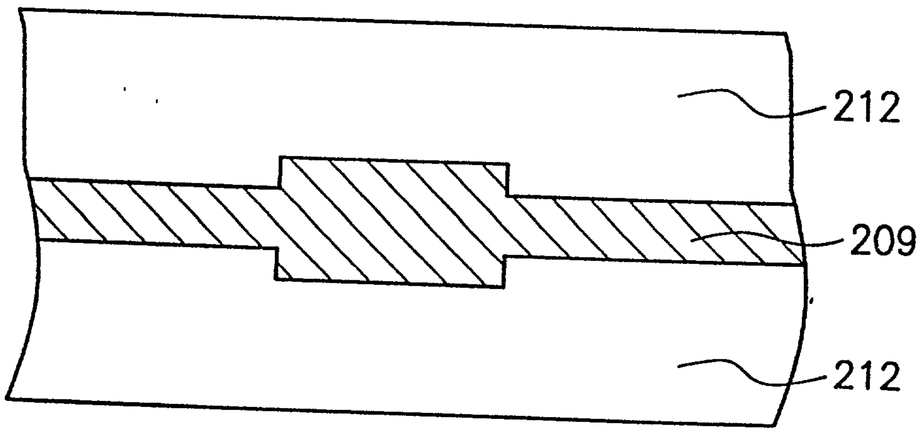


FIG. 3A

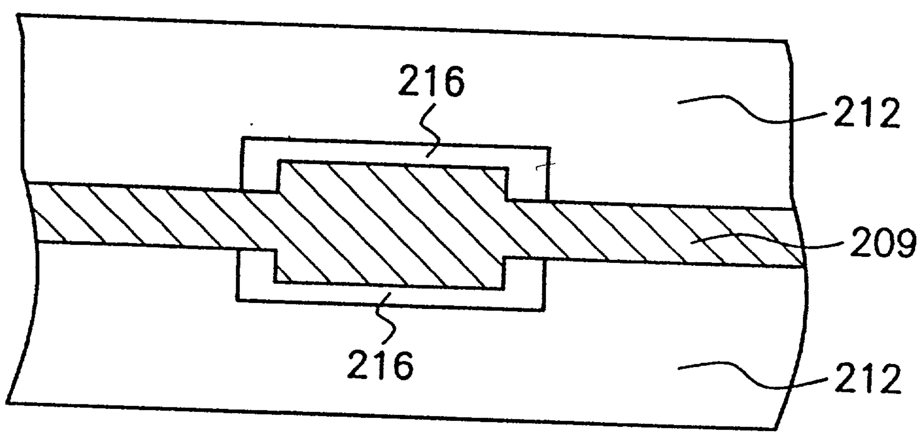


FIG. 3B

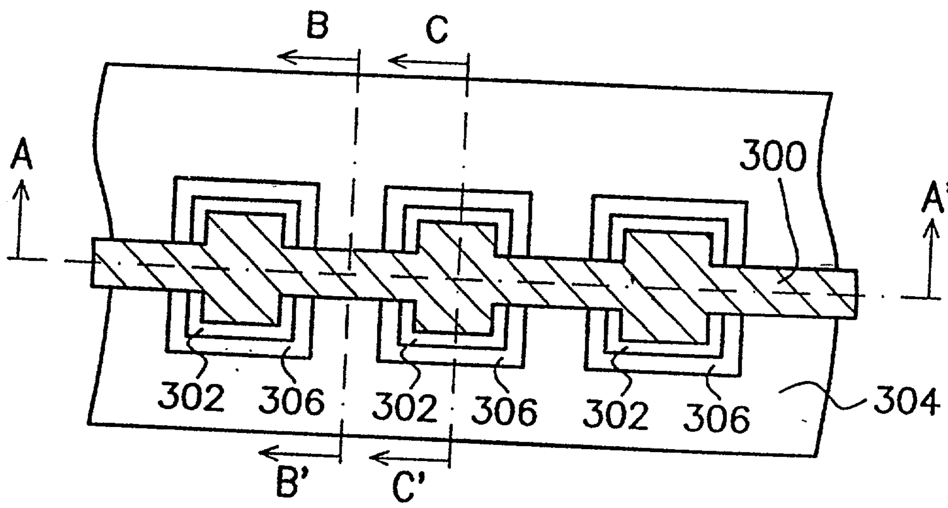
B
C
A
300
A'
302
306
302
306
302
306
304
B'
C'

FIG. 4A

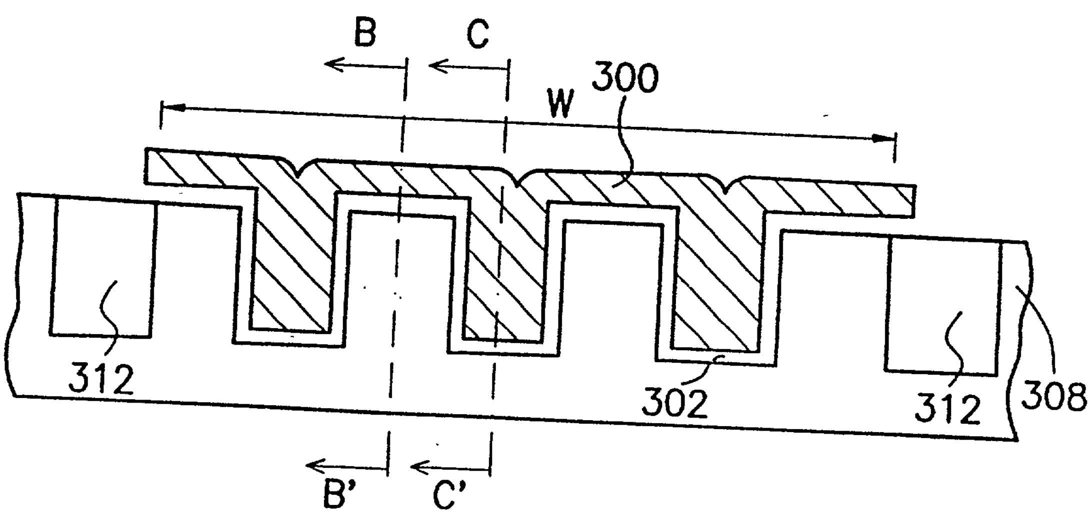
B
C
W
300
312
302
312
308
B'
C'

FIG. 4B

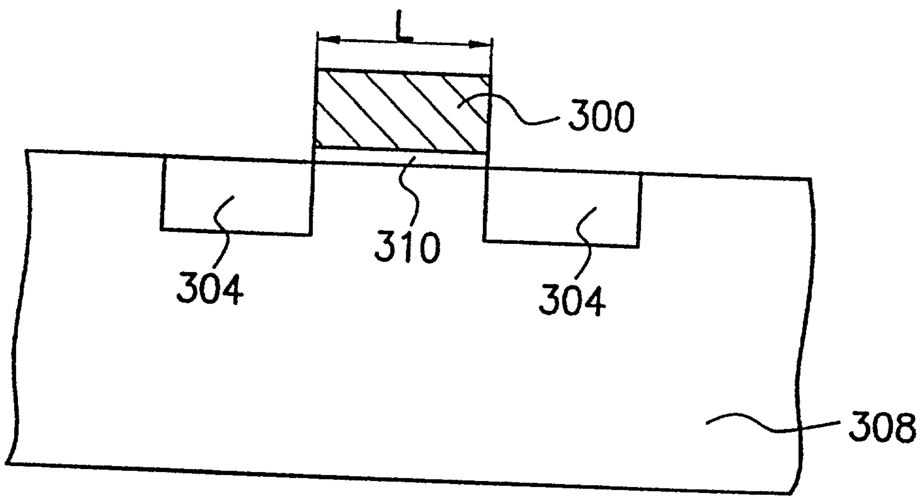


FIG. 4C

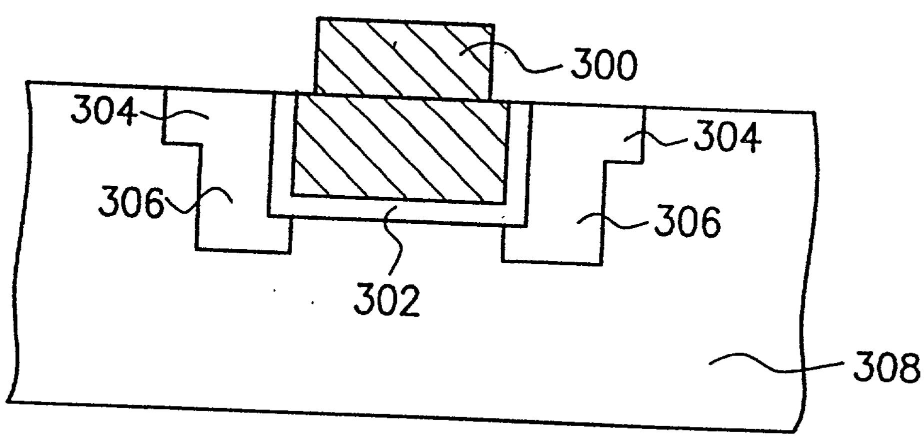


FIG. 4D

Docket No. 2392-US-PA-1C
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | |
|---|---|
| **In Re Application of : Kuan-Yu Fu** | ) |
| **Serial No.: 09/382,146** | ) **Group Art Unit: 2811** |
| **Filed : 1999/8/24** | ) **Examiner: HU, S** |
| **For: MOSFET DEVICE** | ) |

## REVOCATION OF POWER OF ATTORNEY

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

I am an officer of United Microelectronics Corp., authorized to act on behalf of United Microelectronics Corp., the assignee of the entire right, title and interest in the above-referenced application for patent. Evidence of this assignment is recorded in the Patent and Trademark Office at **Reel No.** 9099 **, Frame No.** 0177 . I hereby revoke all previous powers of attorney to prosecute the application and to transact all business connected therewith.

## POWER OF ATTONEY

As an officer of the assignee of the entire right, title and interest in the above-referenced application for patent, I hereby appoint the following attorney(s) and/or Agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

| | | | |
|---|---|---|---|
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| **Maria Erlinda C. Sarno** | **(Reg. No. 37,436)** | **Chanette Armstrong** | **(Reg. No. 44,011)** |
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# COMBIN DECLARATION AND POWER OF . . TORNEY

As the below named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name and that I believe I am an original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

MOSFET DEVICE AND METHOD OF FABRICATING THE SAME

the specification of which

_X_ is attached hereto.
___ was filed on _______________
as Application Serial No.______________ and was amended on_______________.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, Untied States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:
Prior Foreign Application(s):

| Number | Country | Date Filed | Yes | No |
|---|---|---|---|---|
| 87100226 | Taiwan, R.O.C. | January 9, 1998 | X | |
| | | | | |

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

SEE ATTACHMENT

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

Signature: ______________________ Date Jan. 15, 1998

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